REMARKS

The following remarks are fully and completely responsive to the Office Action dated October 1, 2004. Claims 4-10 are pending in this application. By this Amendment, claims 4 and 9 have been amended. In the outstanding Office Action, claims 4-10 were rejected under 35 U.S.C. §103(a). No new matter has been added. Claims 4-10 are presented for reconsideration.

Form PTO-1449

Applicants respectfully note on the Form PTO-1449 filed with the Information Disclosure Statement dated September 29, 2003 and attached to the April 12, 2004 Office Action, the Examiner has not initialed the reference JP 2001297595 cited under Foreign Patent Documents indicating the Examiner has considered the references cited therein. Applicants respectfully request the Examiner consider the reference and provide a copy of Form PTO-1449 with the Examiner's initials next to the cited reference indicating the Examiner properly considered the reference. A copy of the PTO Form 1449 is attached for the Examiner's convenience.

35 U.S.C. § 103(a)

Claims 4-10 were rejected under 35 U.S.C. §103(a) as being unpatentable over Haraguchi (U.S. Patent No. 6,178,127 B1) in view of Lee (U.S. Patent No. 6,735,727 B1). In making this rejection, the Office Action asserts that these references teach and/or suggest every element of the claimed invention. Applicants respectfully submit that claims 4-10 recite subject matter that is neither disclosed nor suggested by the cited prior art.

Claim 4 has been amended to include some of the limitations included in claim 9, which depends directly from claim 4. Claim 4, as amended, recites in part:

> a signal line for connecting the address input circuit and the drive circuit;
>
> ...a supply circuit for supplying information stored in the defective line information store circuit to the redundant circuit via the signal line...

Thus, the signal line that connects the address input circuit to the drive circuit is also used to connect the supply circuit, which supplies information stored in the defective line information store circuit to the redundant circuit. As such, the present invention of claim 4 results in the advantages of simple structure and operation of a semiconductor memory device.

It is respectfully submitted that the prior art fails to disclose or suggest each and every element of Applicants' invention as set forth in claim 4, as amended, and therefore fails to provide the advantages that are provided by the present application.

In rejecting claim 9, the Office Action asserts that Haraguchi teaches a supply circuit for supplying information stored in the defective line information store circuit to the redundant circuit via the signal line. In making this assertion, the Office Action states that defective information from the RAP circuit is supplied to redundant column signal lines via a multiplexer (supply circuit).

In contrast, Haraguchi teaches a defective column address program circuit RAP. This circuit includes address program circuits 70 and 71, which store the respective column address bits of a defective column address. The RAP circuit also includes a redundant enable circuit 72, which stores information indicating whether a redundant column is to be used or not.

The output from the RAP circuit is provided to column decoder 33. The output of the redundant column decoder is provided to a multiplexer 934 for the redundant column.

The line that connects the RAP circuit to the redundant column decoder 933 is not also used to connect the address input circuit to the recited drive circuit. Accordingly, Haraguchi cannot teach and/or suggest "a supply circuit for supplying information stored in the defective line information store circuit to the redundant circuit via the signal line". The signal line recited in this section is recited as "a signal line for connecting the address input circuit and the drive circuit".

The Office Action cites Lee as teaching the recited supply circuit.

Lee, at column 6, beginning at line 5, teaches a redundancy selection circuit 300, which stores addresses, corresponding to defective columns in the main cell array 200. This results in the defective columns being replaced with corresponding redundant bit lines in the redundant cell array 210, during normal read and program modes of operation. Lee also teaches that the redundant selection circuit 300 includes programmed column addresses which allow all redundant memory cells in the array 210 to be selected during a test mode of operation. Accordingly, address information can be freely rewritten in the redundancy selection circuit 300 so that any defective or non-defective cell in the redundant cell array 210 can be selected during the test mode of operation.

Therefore, Lee teaches that the supply circuit for supplying information stored in the defective line information store circuit to the redundant circuit is part of the redundant selection circuit 300. Shown in Figure 4 of Lee, the redundancy selection

circuit 300 outputs a RSi signal to multiplexer 270. In contrast, the row address signal RA is provided to the X decoder 220. Similarly, the column address signal CA is provided to the Y decoder 230. The word line output from the X decoder 220 is provided to the main cell array and redundant cell arrays 200, 210. The output of the Y decoder 230 is provided to the Y-pass gate 240.

As clearly illustrated in Figure 4 and discussed above, the signal from an address input circuit to the drive circuit of Lee is not used to connect the "supply circuit for supplying information stored in the defective line information store circuit to the redundant circuit" as recited in claim 4. Therefore, Lee fails to teach and/or suggest "a supply circuit for supplying information stored in the defective line information store circuit to the redundant circuit via the signal line," the signal line being "a signal line for connecting the address input circuit and the drive circuit".

Accordingly, the combination of Lee and Haraguchi fails to disclose and/or suggest the recited invention. Specifically, the combination of these two references fails to teach and/or suggest "a supply circuit for supplying information stored in the defective line information store circuit to the redundant circuit via the signal line," the signal line being defined as a signal line for connecting the address input circuit to the drive circuit". Therefore, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 4-10 under 35 U.S.C. § 103(a).

Conclusion

Applicants' amendments and remarks have overcome the rejections set forth in the Office Action dated October 1, 2004. Applicants' remarks have distinguished claims

4-10 from the combination of Haraguchi and Lee and thus overcome the rejection of these claims under 35 U.S.C. §103(a). Accordingly, claims 4-10 are in condition for allowance. Therefore, Applicants respectfully request reconsideration and allowance of claims 4-10.

Applicants submit that the application is now in condition for allowance. If the Examiner believes the application is not in condition for allowance, Applicants respectfully request that the Examiner contact the undersigned attorney by telephone if it is believed that such contact will expedite the prosecution of the application.

In the event that this paper is not considered to be timely filed, Applicants hereby petition for an appropriate extension of time. The Commissioner is authorized to charge payment for any additional fees which may be required with respect to this paper to our Deposit Account No. 01-2300, making reference to attorney docket number 107337-00053.

Respectfully submitted,
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Enclosure: Petition for Extension of Time

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